Docket No.: WMP-IFT631

CERTIFICATION

I, the below named translator, hereby declare that: my name and post office address are as stated below; that I am knowledgeable in the English and German languages, and that I believe that the attached text is a true and complete translation of the application filed on August 30, 2001 under Application Number 09/943,589.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Description

Circuit arrangement for detecting the current in a load transistor

The present invention relates to a circuit arrangement having a load transistor and a current sensing transistor coupled to the load transistor in accordance with the features of the preamble of patent claim 1.

In order to detect the current through a load transistor which serves for switching a load, it is known to connect in parallel with the load transistor a transistor as a current sensing transistor which is operated with the same operating point as the load transistor. Figure 1 shows such a circuit arrangement, also referred to as a current sense arrangement, according to the prior art.

The circuit arrangement has a load transistor T1S, which is connected up in series with a load Z1S between a supply potential Vdd and a reference-ground potential GND. Arranged in parallel with the load transistor T1S is a current sensing transistor T2S, whose gate terminal is connected to the gate terminal of the load transistor T1S and whose drain terminal

together with the drain terminal of the load transistor T1S is connected to a supply potential Vdd. A series circuit comprising a transistor T3S and a current sensing resistor Z2S is connected downstream of the source terminal of the current sensing transistor T2S. In this case, the transistor T3S is driven by means of a comparator K1S, which compares the source potentials of the load transistor T1S and of the current sensing transistor T2S with one another in order to set them to the same value. The current I2 through the current sensing transistor T2S is then proportional to the current I1 through the load transistor T1S, the ratio of these two currents depending on the ratio of the dimensions of the load transistor T1S and of the current sensing transistor T2S.

It is also known for a current supplied by a current sensing transistor in accordance with figure 1 to be fed to different application circuits than that illustrated in figure 1. In this case, in known circuit arrangements, a dedicated current sensing transistor is provided for each of the evaluation circuits.

The load transistor and the associated current sensing transistor are usually integrated in a chip, while evaluation circuits are integrated in a further chip. In this case, a line connection is required between each of the current sensing transistors in one chip and the associated processing

circuit in the other chip, which means that each of these connections requires a contact pin on the first and second chips.

It is an aim of the present invention to provide a circuit arrangement for evaluating the load current of a load transistor which can be realized simply with known circuit means and in which, in particular, the abovementioned disadvantages do not occur.

This aim is achieved by means of a circuit arrangement in accordance with the features of patent claim 1.

The subclaims relate to advantageous refinements of the invention.

The circuit arrangement according to the invention has a load transistor and a current sensing transistor coupled to the load transistor, wherein a switch arrangement having at least one first switch is connected downstream of the current sensing transistor in order to connect the current sensing transistor to a first or second evaluation circuit depending on a control signal.

The circuit arrangement according to the invention requires only one current sensing transistor, whose output current can

be fed via the switch arrangement as required to one of the evaluation circuits.

In accordance with one embodiment of the invention, it is provided that the switch arrangement can be driven depending on a load path voltage (drain-source voltage) of the load transistor. It is thus possible to provide, as an evaluation circuit, circuit components which supplement the current sensing resistor to form a conventional current sense circuit according to figure 1, the current of the current sensing resistor being fed to this evaluation circuit only until a predetermined drain-source voltage of the load transistor is reached. Conventional current sense circuits supply a current signal which is proportional to the load current only when the load transistor is not yet in saturation, in other words when the drain-source voltage is below a saturation voltage. By means of the circuit arrangement according to the invention, the current of the current sensing resistor can be fed to another evaluation circuit when the drain-source voltage reaches the value of the saturation voltage and the current of the current sensing resistor can no longer be suitably evaluated anyway in the current sense arrangement.

In accordance with a further embodiment of the invention, it is provided that the load transistor and the current sensing transistor are integrated in a first chip, and that the switch

arrangement and the first and second evaluation circuits are integrated in a second chip. In this embodiment of the invention, only one line connection is required between the first chip and the second chip in order to be able to feed the load current of the current sensing resistor to the evaluation circuits.

The present invention is explained in more detail below using exemplary embodiments with reference to figures, in which:

Figure 1 shows a current sense arrangement according to the prior art;

Figure 2 shows a circuit arrangement according to the invention in accordance with one embodiment of the invention;

Figure 3 shows a circuit arrangement according to the invention in accordance with figure 2 with a detailed illustration of the switch arrangement and of an exemplary embodiment of the first and second processing units.

In the figures, unless specified otherwise, identical reference symbols designate identical structural parts with the same meaning.

Figure 2 shows an exemplary embodiment of the circuit arrangement according to the invention. The circuit arrangement has a load transistor T1 and a current sensing transistor T2, which are designed as n-channel MOS transistors in the exemplary embodiment. A drain terminal D of the load transistor T1 and a drain terminal D of the current sensing transistor T2 are connected to a supply potential Vdd. A gate terminal of the load transistor T1 and a gate terminal of the current sensing transistor T2 are jointly connected to an input terminal IN for feeding in a drive signal, according to which the load transistor (and the current sensing transistor) turns on or turns off. The load transistor T1 and the current sensing transistor T2 are preferably integrated in a semiconductor body which has a multiplicity of identically constructed transistor cells, some of the transistor cells (usually the majority) being connected to one another in order to form the load transistor T1 and some of the transistor cells (usually a small portion) being connected to one another in order to form the current sensing transistor T2. A load Z_L is connected between a source terminal S of the load transistor T1 and a reference-ground potential GND, which load is driven by means of the load transistor T1. The source terminal S of the current sensing transistor T2 is connected to a switch arrangement SW, which connects the source terminal S to a first or a second evaluation unit BL1, BL2 depending on a switch position of a switch S1. This switch arrangement SW

has a first comparator K1 as comparator unit, one of whose terminals is connected to the source terminal S of the load transistor T1 and whose other terminal is connected to the supply potential Vdd via a reference voltage source Uref.

An output signal of the comparator K1 assumes an upper drive level if a drain-source voltage UDS1 across the drain-source path D-S of the load transistor T1 is greater than the reference voltage Uref, and the output signal AS assumes a lower drive level if the drain-source voltage UDS1 is less than the reference voltage Uref. The switch S1 driven by the drive signal AS connects the first evaluation circuit BL1 or the second evaluation circuit BL2, depending on the level of the drive signal AS, to the source terminal S of the current sensing transistor T2 in order to feed the load current of the current sensing transistor T2 to the first or second evaluation circuit.

The load transistor T1 and the current sensing transistor T2 are preferably integrated in a first chip IC1, while the switch arrangement S and the drive circuits BL1, BL2 are preferably integrated in a second chip IC2. The load current I_s of the current sensing transistor T2 is available at a first terminal pin P11 of the first chip IC1 and is fed to the second chip IC2 via a terminal pin P21. In this case, the terminal pins P11, P21 are connected to one another by means

of a bonding wire BD. The usually external load Z_L is connected to a second terminal pin P12 of the first chip IC1. In this case, the second input of the comparator K1 can likewise be connected to said second terminal pin P12, and so this does not require a separate connection between the first chip IC1 and the second chip IC2. The second chip IC2 has a dedicated terminal pin (not specifically illustrated) for the supply potential Vdd, and so the first terminal of the comparator K1 does not have to be connected via the reference voltage source Uref to the supply potential Vdd in the first chip IC1, which is illustrated in this way in figure 2 merely for reasons of clarity.

Figure 3 shows an exemplary embodiment of the circuit arrangement according to the invention, in which an exemplary embodiment of the construction of the first evaluation circuit BL1 and of the second evaluation circuit BL2 is respectively illustrated.

The first evaluation circuit BL1 supplements the current sensing transistor T2 in the example to form a current sense circuit. The evaluation circuit BL1 has a regulating transistor T3 which is connected in series with the current sensing transistor T2 via the terminal pins P21, P11 of the first and second chips IC1, IC2. A current sensing resistor Rs is connected between the regulating transistor T3 and

reference-ground potential GND. The regulating transistor T3, which is designed as a p-channel transistor in the exemplary embodiment, is driven by a second comparator K2, whose first input (inverting input) is connected to the terminal pin P21 of the second chip IC2 and to the source terminal S of the current sensing transistor T2. A second input (noninverting input) of the second comparator K2 is connected to the second pin P12 of the first chip IC1 and to the source terminal S of the load transistor T1. The second comparator K2 regulates the resistance of the drain-source path of the regulating transistor T3 in such a way that the source potential of the load transistor T1 and the source potential of the current sensing transistor T2 correspond, with the result that the load transistor T1 and the current sensing transistor T2 are operated with the same operating point. The load current I_s of the current sensing transistor T2 is then proportional to the load current I_L of the load transistor T1.

A voltage signal Is1 can be tapped off at the current sensing resistor RS, which voltage signal is proportional to the current sense current I_s or the load current I_L of the load transistor T1.

The switch arrangement S in accordance with figure 3 has, in addition to the comparator K1, first and second transistors S1a, S1b which are designed as p-channel transistors and whose

gate terminals G are connected to the output of the comparator K1. Source terminals S of the first and second transistors S1a, S1b are connected to the supply potential Vdd. The drain terminal of the first transistor S1a is connected to the gate G of the regulating transistor T3. If the first transistor S1a turns off, then the arrangement comprising the comparator K2, the transistor T3 and the current sensing resistor RS functions in the manner described above. If the first transistor S1a turns on, then the gate of the third transistor T3 is connected to supply potential Vdd, as a result of which the third transistor T3 turns off, so that the load current I_s no longer flows through the current sensing resistor RS and the current signal Us1 falls to zero. The first transistor S1a and the second transistor S1b are in the on state as long as the drain-source voltage UDS1 of the load transistor T1 is less than the reference voltage Uref.

Current sense arrangements like those produced from the circuit arrangement of the evaluation circuit BL1 according to figure 3 and the current sensing resistor T2 function with sufficient accuracy, that is to say supply a voltage signal Is1 which is proportional to the load current I_L, only when the load transistor T1 is not yet in saturation, in other words as long as the load current I_L rises proportionally to the drain-source voltage UDS1.

If the drain-source voltage UDS1 of the load transistor T1 exceeds the value of the reference voltage Uref, which is preferably chosen such that it is less than the saturation voltage of the load transistor T1, then the load current I_s can be switched over to the second evaluation circuit by means of the switch arrangement SW. This ensures that a current signal Us1 is generated by the first evaluation circuit BL1 only as long as the load transistor T1 is not yet in saturation and as long as the current sense arrangement can supply a signal Us1 which is proportional to the load current of the load transistor T1.

The second evaluation circuit BL2 has a series circuit comprising a resistor R2 and an n-channel transistor T4, this series circuit likewise being connected to the terminal pin P21 of the second chip IC2. The gate terminal G of the transistor T4 is connected to the source terminal of the transistor S1b of the switch arrangement and connected to reference-ground potential GND via a resistor R1. If the second transistor S1b turns on, then approximately the entire supply voltage Vdd is present across the resistor R1, as a result of which the transistor T4 turns on. The transistor T4 turns off if the second transistor S1b also turns off. The fourth transistor T4 thus turns on when the regulating transistor T3 turns off and the fourth transistor T4 turns off when the regulating transistor T3 turns on. This ensures that

the load current I_s of the current sensing resistor T2 flows either only into the first evaluation circuit BL1 or only into the second evaluation circuit BL2.

The first evaluation circuit BL1 supplies a signal Us1 proportional to the load current L_L as long as the load transistor T1 is not yet in saturation or as long as the drain-source voltage UDS1 is less than the reference voltage ref. If the drain-source voltage UDS1 exceeds the reference voltage Uref, then the load current I_s of the current sensing transistor T2 flows into the second evaluation circuit BL2, where this load current I_s generates across the second resistor R2 a voltage drop Us2 which can be used as second current signal Us2 for setting the drive voltage (gate-source voltage) of the load transistor T1. The load current of the load transistor T1 and thus also the load current of the current sensing transistor T2 are greatly dependent on the gate-source voltage in the saturation region. Depending on the load current of the current sensing resistor T2, the gate-source voltage of the load transistor can then be set by way of the current signal Us2. The second drive circuit BL2 may be used, in particular, as part of a current limiting circuit which reduces the gate-source voltage of the load transistor T1 if the load current exceeds a predetermined value, which can be determined from the voltage signal Us2.